

LISTING OF CLAIMS

1. (Previously Presented) A CMOS imager, comprising:

a photoconversion device;

a transfer transistor, said transfer transistor comprising a transfer gate with a first side and a second side opposite said first side, said transfer gate being associated with said photoconversion device at said first side of said transfer gate;

a reset transistor at said second side of said transfer gate, said reset transistor comprising a reset gate; and

a floating diffusion region at said second side of said transfer gate, between said transfer gate and said reset gate, said floating diffusion region comprising an active area extension region at said second side of said transfer gate and a halo implant region below said active area extension region, wherein said floating diffusion region is closer to said reset gate than to said transfer gate.

2. (Cancelled).

3. (Cancelled).

4. (Previously Presented) The CMOS imager of claim 1, wherein said transfer transistor has an underlying channel region, said channel region having a threshold voltage adjustment implant.

5. (Previously Presented) The CMOS imager of claim 1, wherein said transfer transistor has a gate length which is greater than that of all other transistors of a same pixel cell.

6. (Previously Presented) The CMOS imager of claim 1, wherein said halo implant region extends partially below the transfer gate.

7. (Original) The CMOS imager of claim 1, wherein said photoconversion device is one of a photodiode, a photogate, or a photoconductor.

8. (Currently Amended) The CMOS imager of claim 1, wherein said active area extension region and said halo implant region are laterally spaced away from the transfer gate by a portion of a substrate supporting said first transistor and ~~including~~ said active area extension region.

9. (Previously Presented) The CMOS imager of claim 1, wherein said photoconversion device is part of a four transistor pixel circuit comprising said transfer transistor, said reset transistor, a source follower transistor, and a row select transistor.

10. (Original) The CMOS imager of claim 9, wherein at least one of said reset transistor and said source follower transistor have a single active area extension region.

11. (Cancelled).

12. (Cancelled).

13. (Previously Presented) The CMOS imager of claim 1, wherein said active area extension region at said second side of said transfer gate has a dopant concentration of about  $1 \times 10^{12}$  to about  $3 \times 10^{13}$  ions/cm<sup>2</sup>.

14. (Previously Presented) The CMOS imager of claim 1, wherein said transfer transistor has a single insulating spacer, said spacer positioned on said second side of said transistor gate and over said active area extension region and said halo implant.

15. (Previously Presented) A pixel sensor cell, comprising:

a semiconductor substrate;

a transfer transistor over said substrate, said transfer transistor having a single active area extension region located on a first side of said transfer transistor;

a photosensor in electrical communication with said transfer transistor, said photosensor being within said substrate on a second side of said transfer transistor which is opposite to said first side;

a reset transistor gate over said substrate and spaced apart from said transfer transistor; and

a floating diffusion region on the first side of said transfer transistor and adjacent said reset transistor gate, said floating diffusion region being in electrical communication with said active area extension region and comprising a halo implant region below said single active area extension region and an n-type doped region at the surface of said substrate and spanning said floating diffusion region and said single active area extension region.

16. (Previously Presented) The pixel sensor cell of claim 15, wherein said transfer transistor has a threshold voltage adjustment implant in said substrate below a gate of said transfer transistor.

17. (Previously Presented) The pixel sensor cell of claim 15, wherein said transfer transistor has a gate length which is greater than that of all other transistor gates of said pixel sensor cell.

18. (Original) The pixel sensor cell of claim 15, wherein said reset transistor comprises two active area extension regions as lightly doped drains on opposite sides of said reset transistor gate.

19. (Original) The pixel sensor cell of claim 15, wherein said reset transistor comprises a single active area extension region on a side opposite said floating diffusion region.

20. (Original) The pixel sensor cell of claim 15, further comprising at least a source follower transistor and a row select transistor.

21-25. (Cancelled).

26. (Previously Presented) An image sensor, comprising:

a semiconductor substrate;

a transfer gate over said substrate;

a reset gate over said substrate, wherein said transfer gate has a gate length greater than that of said reset transistor;

a floating diffusion region in said substrate and between said transfer gate and said reset gate, said floating diffusion region being closer to said reset gate than to said transfer transistor gate;

a single active area extension region in said substrate adjacent to said transfer gate and said floating diffusion region;

a halo implant region in said substrate below said single active area extension region;

an n-type surface layer over said floating diffusion region and said single active area extension region;

a threshold voltage implant in said substrate below said transfer gate; and

a photodiode adjacent said transfer gate at a side opposite said active area extension region and said floating diffusion region.

27. (Original) The image sensor of claim 26, wherein the image sensor is a CMOS imager.

28. (Previously Presented) The image sensor of claim 26, wherein said floating diffusion region and said single active area extension region are laterally separated from said transfer gate in a direction toward said reset gate by a portion of said substrate.

29. (Previously Presented) The image sensor of claim 26, further comprising a source follower gate and a row select gate.

30. (Previously Presented) The image sensor of claim 29, wherein at least one of said reset gate, said source follower gate, and said row select gate are associated with a second single active area extension region.

31. (Previously Presented) The image sensor of claim 29, wherein said transfer gate has a gate length greater than that of said source follower gate and said row select gate.

32. (Previously Presented) An imager device, comprising:

an image processor; and

a pixel array for supplying signals to said image processor, at least one pixel of said array comprising:

a photoconversion device;

a first transistor gate associated with said photoconversion device at a first side of said transistor gate, said gate having a length which is greater than that of all other transistor gates of said pixel;

a single lightly doped drain on a second side of said transistor gate opposite said first side;

a channel region under said transistor gate and comprising a threshold voltage adjustment implant; and

a halo implant below said lightly doped drain.

33. (Previously Presented) The imager device of claim 32, further comprising a surface n-type layer over said lightly doped drain.

34. (Original) The imager device of claim 32, wherein said first transistor gate is of a transfer transistor in electrical communication with said photoconversion device.

35. (Cancelled).

36. (Cancelled).

37. (Original) The imager device of claim 32, wherein said photoconversion device is a photodiode.

38. (Currently Amended) An integrated circuit, comprising a transistor in electrical contact with a photodiode, said transistor comprising a single active area extension region on a side of said transistor opposite from said photodiode, a halo implant below said single active area extension region, an n-type layer over said single active area extension region, and a threshold voltage implant below said transistor, wherein said transistor has a gate length that is greater than that of any other transistor of a same pixel.

39. (Currently Amended) The integrated circuit of claim 38, further comprising a floating diffusion region adjacent a gate of said transistor, said single active area extension region and said halo implant ~~being a~~ overlapping at least part of said floating diffusion region.

40. (Cancelled).

41. (Previously Presented) The integrated circuit of claim 38, wherein said active area extension region and said floating diffusion region are laterally spaced away from a gate of said transistor by a portion of a substrate supporting said transistor.

42. (Previously Presented) The integrated circuit of claim 38, further comprising an insulating layer over said transistor and said photodiode, said insulating layer extending to a floating diffusion region adjacent to said active area extension region.

43. (Previously Presented) The integrated circuit of claim 38, wherein said transistor and said photodiode are part of a CMOS imager pixel.

44. (Withdrawn) The integrated circuit of claim 38, wherein said transistor and said photodiode are part of a CCD imager.

45. (Previously Presented) The integrated circuit of claim 38, wherein said transistor is part of a pixel having at least two other transistors in electrical communication with said photodiode.

46. (Currently Amended) A pixel cell, comprising a transistor in electrical contact with a photodiode, said transistor comprising a single active area extension region and halo implant region on a opposite side of said transistor from said photodiode, said transistor also having a gate length which is ~~increased relative to~~ greater than that of any other transistor ~~gate length of transistors~~ of a same pixel.

47. (Cancelled).

48. (Previously Presented) The pixel cell of claim 46, comprising a threshold voltage adjustment implant below a gate of said transistor.

49. (Previously Presented) The pixel cell of claim 46, comprising a source/drain region adjacent to said active area extension region, said active area extension region and said source/drain region being spaced away from a gate of said transistor by a portion of a substrate supporting said transistor.

50-93. (Cancelled).